REMARKS

The present invention is a transceiver interface connectable in use to a cable. An embodiment of an interface in accordance with the invention includes an input as illustrated in Fig. 5 receiving a pair of signals D+ D- and logic circuit 18 connected to the input having a single logic output line 21, wherein the single logic output line of the logic circuit has a first output state where both signals are below a predetermined level and a second output state where either or both signals exceed the predetermined level. The present invention replaces the use of Schmitt triggers 14 and 15 for producing the pair of outputs 16 and 17 with a logic circuit which in a preferred embodiment is a NOR gate 18 as illustrated in Fig. 5. The present invention reduces the number of logic outputs from two to one which simplifies the complexity of the transceiver bus interface to perform in accordance with the USB standard.

Claims 1-8 and 10-17 stand rejected under 35 USC §102 as being anticipated by United States Patent 6,615,301 (Lee et al.). This ground of rejection is traversed for the following reasons.

Lee et al. discloses the same subject matter as the admitted prior art in Fig. 4. Claim 1 differs from the subject matter of Lee et al. and the admitted prior art of Fig. 4 in that claim 1 recites "a transceiver interface connectable, in use to a cable, the interface including an input for receiving a pair of signals from said cable, and a logic circuit connected to the input having a single logic output line wherein the single logic output line of the logic circuit has a first output states where both signals are below a predetermined level and a second output state where either or both signals

exceed the predetermined level". The identity of the admitted prior art of Fig. 4 of the present application with Lee et al. is seen from Figs. 3 and 4 of Lee et al., in which the inputs 343 and 344, which are DM and DP, respectively, correspond to the bus inputs D+ and D- of the admitted prior art. Three outputs 346, 347 and 348 are produced with two of the outputs being logic signals.

Fig. 4 of Lee et al. shows an implementation of the bus receiver 310, with the output 347 being a differential signal produced by differential amplifier 411 and the outputs 346 and 348 being produced by Schmitt triggers 421 and 421' which correspond to Schmitt triggers 14 and 15 of the admitted prior art of Fig. 4. The outputs RXDP and RXDM correspond to the outputs 16 and 17 of the admitted prior art of Fig. 4 with the output RXD corresponding to the differential output 13 produced by differential amplifier 12 of the admitted prior art of Fig. 4.

Moreover, there is no basis in the record why a person of ordinary skill in the art would be led to modify Lee et al., which has the conventional three outputs of the admitted prior art of Fig. 4, to arrive at the subject matter of claim 1 which requires the single logic output line to provide the first and second output states.

It is noted that the Examiner has relied upon NOR gates 62, 623 and 624 in the rejection of claim 2. However, NOR gate 62 is part of the output drive logic 425 illustrated in Fig. 5B which is shown in block diagram form in Fig. 4 which does not satisfy the limitations of claim 1. Moreover, NOR gates 622-624 are part of an active filter of Figs. 5A and 5B. Accordingly, Lee et al. does not disclose the subject matter of claim 2 wherein the logic circuit of claim 1 is recited as a NOR gate.

Moreover, the subject matter of dependent claims 3-8 and 10-17 is also not disclosed.

Newly submitted claim 18 defines a transceiver interface connectable, in use, to a cable, the interface including an input for receiving a pair of signals from said cable, and a logic circuit connected to the input having only a single logic output line wherein the logic circuit has a first output state wherein both signals are below a predetermined level and a second output state where either or both signals exceed the predetermined level. This subject matter is different than the prior art three signal outputs of Lee et al. as illustrated in Fig. 3 where the two logic signal outputs are provided. Moreover dependent claims 19-21 define further aspects of the subject matter of claim 18 which is not anticipated or rendered obvious by Lee et al.

The specification has been amended to improve its form for reexamination including on page 3 to improve the description of the prior art of Fig. 4.

In view of the foregoing amendments and remarks, it is submitted that each of the claims in the application is in condition for allowance. Accordingly, early allowance thereof is respectfully requested.

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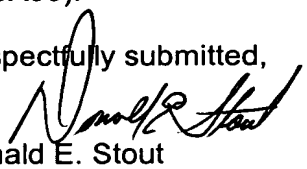
deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (referencing case no. 367.39780X00).

Respectfully submitted,



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